Assembly Technique for a Fine-Pitch, Low-Noise Interface; Joining a CdZnTe Pixel-Array Detector and Custom VLSI Chip with Au Stud Bumps and Conductive Epoxy

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***Abstract*--Energy resolution of hard x-ray detectors can be adversely affected by the input capacitance between the CdZnTe anodes and VLSI readout chip or substrate. This problem is compounded with minimal separation distances between planes that are on the order of 8-10 microns using typical Indium Bump Bonding methods. A improved technique is presented and compared that increases the separation between planes by adhesively-bonding single or stacked gold stud bumps, thermosonically bonded on an array of pads of a custom VLSI chip, with silver-filled conductive epoxy that is stencil printed on the anode contacts of the CdZnTe detector. This technique uses low-force and low-temperature processing and can be adapted to avoid direct contact between the conductive epoxy and VLSI surface. The assembly of a 24 X 44, 500-micron pitch, pixel array is detailed in this report. This sensor packaging technique is presently being evaluated for the balloon-launched, High Energy Focusing Telescope (HEFT) experiment at the California Institute of Technology.**

I. INTRODUCTION

Large area CdZnTe detectors are becoming the material of choice for applications ranging from near-space, in the form of medical imaging devices, to deep-space hard x-ray and gamma ray sensors. This material is characterized by excellent photoabsorption efficiency, low leakage at or even slightly above room temperature and good energy resolution [1]. Many of these sensors employ fine-pitched pixel arrays with very high pin counts - in excess of 1000 interconnections - that are flip chip mounted to custom application-specific integrated circuit (ASIC) readout chips. Since CdZnTe detectors are limited to processing temperatures below 100°C, conventional solder flip chip assembly is not a practical option. There are only two flip chip assembly techniques presently in widespread usage that would qualify as low-temperature processes: indium bump bonding and adhesive bonding using conductive (isotropic) epoxy. Indium bump bonding has been and remains the primary means for assembling these high-density detectors, but is an expensive process. Adhesive bonding is less expensive, but is currently limited to pad pitches >100µm (microns). This later process consists of joining conductive epoxy bumps, stencil printed on the detector, with gold (Au) stud-bumps thermosonically bonded to the ASIC chip pads. An opportunity to compare the performance of these two flip chip mounting techniques, using identical pad pitches and ASIC readout chips, was provided during the development of the detectors designed for the High Energy Focusing Telescope (HEFT) balloon experiment at the California Institute of Technology. The results of this comparison indicate that the higher standoff height provided by the Au-stud bumps enables the anode plane design to be optimized for lower leakage current (noise).

II. INDIUM BUMP BONDING (*HYBRIDIZATION*)

Indium bump bonding (or "*hybridization*", as it is commonly called) is the prevailing ultra fine-pitch, flip chip assembly methodology. Several government and private research labs are capable of performing this process at pitches as small as 50µm and the current '*state of the art*' is closer to 18-20µm pitch.

The process begins with vacuum deposition of an Under Bump Metallization (UBM) layer over the metal pads of both surfaces to be joined to prevent diffusion

of the indium. Pure indium metal is then e-beam (vapor) deposited onto the UBM metal using either a shadow mask or photoresist lift-off technique to define the bump geometries. The indium bumps are typically only 15-20µm in diameter and 7-10µm thick at these pitches, resulting in the surfaces being separated by only 8-15µm after assembly. Flatness of the surfaces and uniformity of the indium bump heights are therefore critical to the success of this process.

Unlike solder bump deposition, the indium bumps are not reflowed prior to assembly, leaving their morphology somewhat jagged in appearance (see Fig. 1). This "jagged" topology presumably aids in the joining process by enabling the top surfaces of the bumps to be more deformable and likely to rub through non-conductive surface oxides during the cold or low-temperature fusion process.

Bump to bump interconnection is achieved by aligning the bumps and applying high normal forces (1-2 grams/bump) to cause the bumps on opposing surfaces to fuse (cold-weld) together. Large focal plane arrays with fine-pitched bumps may require several Newton's force to achieve reliable interconnects, creating the potential for damaging delicate CZT detectors. Adding heat to the process renders the indium bumps more malleable, such that less force may be required, but can also introduce residual strain and the potential for shear-fractures developing in the joined bumps after the parts cool to room temperature. Small variation in camber between the mounted surfaces can also cause the indium bumps to separate after removal of the normal forces applied during the fusion process. Consequently, there is an effort underway to try to increase indium bump-heights without compromising the ability to deposit finer-pitched bumps. Since these image sensors cannot typically operate properly with an epoxy underfill present, either the materials being joined must be closely matched for coefficient of thermal expansion (CTE), and/or the joining process must be performed as close to room temperature as possible - especially, since many of these devices are intended to be operated at sub-zero temperatures.

Electroplated solder bumps compare favorably with evaporated indium bumps and can be deposited at pitches as small as 20µm. Solder alloys that can be easily electroplated, however, require reflow temperatures exceeding 212°C [2], and with the industry mandate to eliminate all lead from solder, the processing temperatures have now risen as high as 260°C.

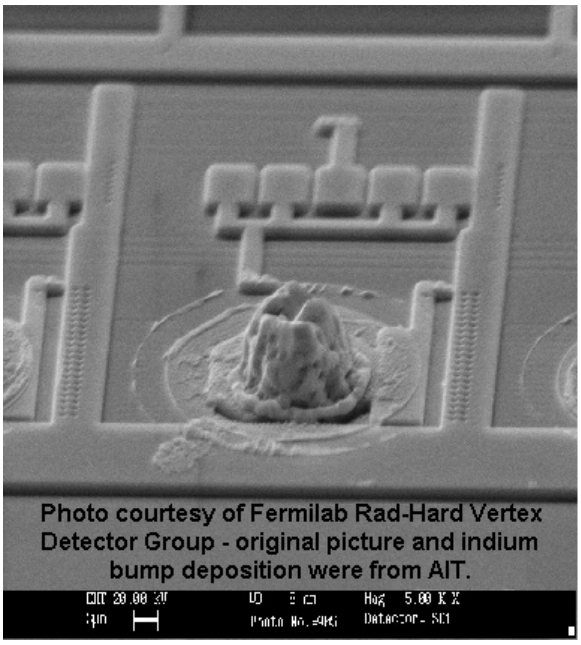

Fig. 1. SEM photo of a vacuum-deposited indium bump (~15-20µm diameter).

III. STENCIL PRINTED POLYMER BUMPING

An alternative "*adhesive*" flip chip assembly process uses silver-filled (isotropic) conductive epoxy. The epoxy is applied directly onto the detector pads using a stencil printing technique. The epoxy-bumped detector is then aligned and lightly pressed against the Au-stud bumps disposed on the ASIC chip until the Au-bumps fully penetrate the wet epoxy. In this manner the Au-stud bumps act as a mechanical stop, preventing the epoxy from over-spreading and causing electrical shorts between adjacent bumps. Prior to assembly the stencil printed polymer bumps resemble a rounded volcano, as shown in Fig. 2. The broad base provides a robust electrical contact on the detector pads but limits the minimum pitch between printed bumps. As a rule of thumb, the epoxy bump diameter is approximately 2-3X larger than the bump height, depending on how thixotropic the epoxy is.

As with indium bump bonding, the uniformity of the Au-stud bump and stencil printed bump height are also critical when working with conductive epoxies for flip chip assembly. If the Au-stud bumps are not of equal height above the chip's surfaces, they may not reach far enough to contact the epoxy and ensure reliable electrical contact. The stencil printing method is more tolerant of Au-stud bump height variation, since the chip's highest bumps typically penetrate the full thickness of the printed epoxy bumps until they touch the underlying pads.

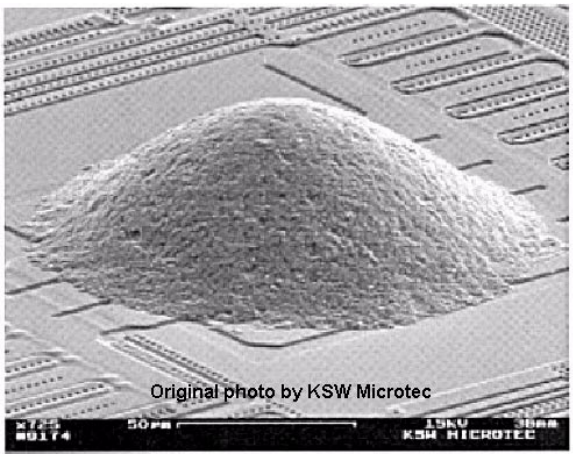

Fig. 2. Stencil printed, conductive epoxy bump (~150µm diameter).

IV. DIE AND WAFER BUMPING OPTIONS

Au-stud bumps are simply modified thermosonic wirebond connections in which the wire has been purposely severed from the ball-bond, leaving only the Au-ball (*stud-bump*) attached to the chip's bond-pad. A major advantage of this technique is that the thermosonic ball-bonding process scrubs through the aluminum oxides present on typical IC pads, eliminating the need to pre-apply any UBM layer. Reliable low-impedance, metal-to-metal interconnects are a distinct characteristic of this technology and a principle reason why wirebonding has remained in favor for so long. Solder and conductive epoxies, conversely, require a compatible metal surface for reliable connections. Silver-filled conductive epoxies perform best in contact with noble metal-finishes such as Au, Ag, Pt or Pd, but will not provide a reliable connection in direct contact with untreated aluminum.

Gold-stud bump bonding is ideal when only a few devices need to be bumped, but is not a particularly efficient process when attempting to bump an entire wafer. Depending on the number of contacts per device, a single wafer may require 8-12 hours of bonder time. Nevertheless, the process is extremely clean and relatively economical, since no chemicals are involved and so little material is consumed in forming the individual ball bumps.

Ensuring a uniform height for every bump within a large array of Au-stud bumps requires control of the diameter of the ball bumps and amount of wire ("*pig-tail*" length) that protrudes from the top of the ball bump. Simply pulling the wire until it breaks does not ensure a repeatable process (see Fig. 3). A better method employs a shearing tool and/or coining technique immediately after the ball bump is thermosonically welded to the pad to establish a more consistent ball bump height [3]. Alternatively, a laser

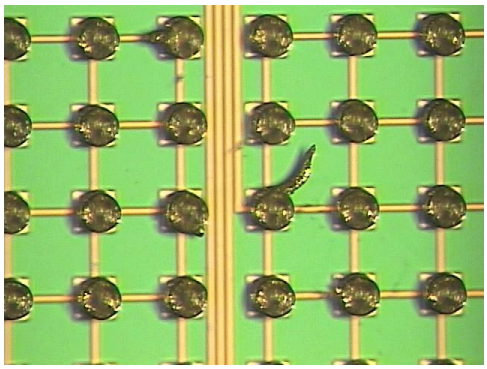

Fig. 3. Photo of Au-stud bumps with protruding wires.

may be employed to cut the wire at a uniform length above the ball bond.

Improved placement accuracy now enables multiple Au-stud bumps to be stacked atop one another to increase the 'stand-off' height. Fig.'s 4 and 5 illustrate examples of double and triple ball bumps bonded directly on top of each other. The triple stud bump measures in excess of 100µm in height with bump-to-bump uniformity reportedly held to within 5-7µm, well within the process window for working with stencil printed conductive adhesives. This extra height aids in decoupling some of the residual strain resulting from coefficient of thermal expansion (CTE) mismatch between the materials being joined and simplifies the under-filling process for large-area devices. It also provides a better low-noise interface for some applications, as discussed below.

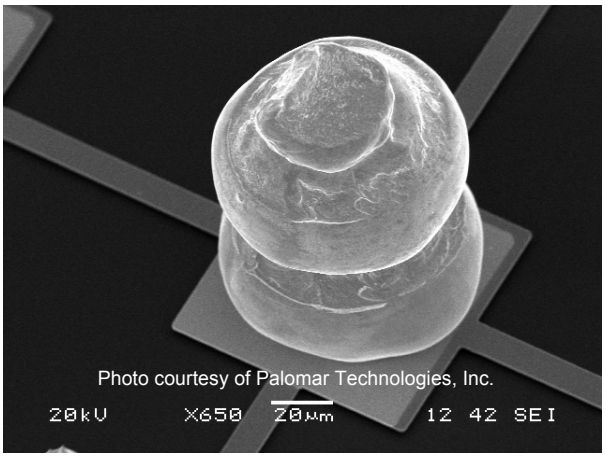

Fig. 4. SEM Photo of a double-ball Au-stud bump.

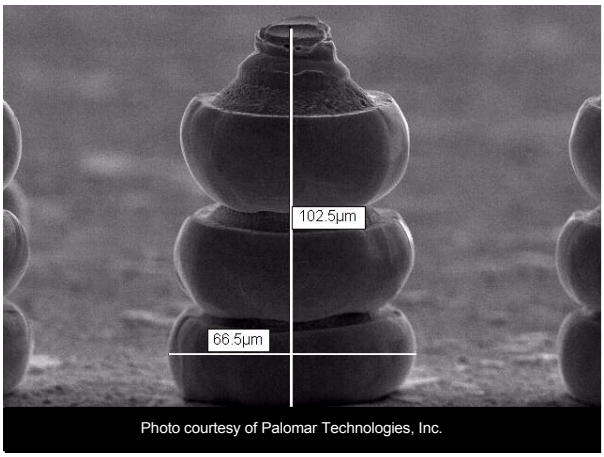

Fig. 5. SEM Photo of a triple-ball Au-stud bump.

A more economical bumping process when handling whole wafers is electroless-plated nickel-gold (Ni-Au) bumps. This process typically deposits between 5-25µm of Ni over the aluminum pads through a zincate process after etching away the surface oxides. A thin Au coating is then plated over the Ni to prevent oxidation of the Ni-bumps (see Fig. 6).

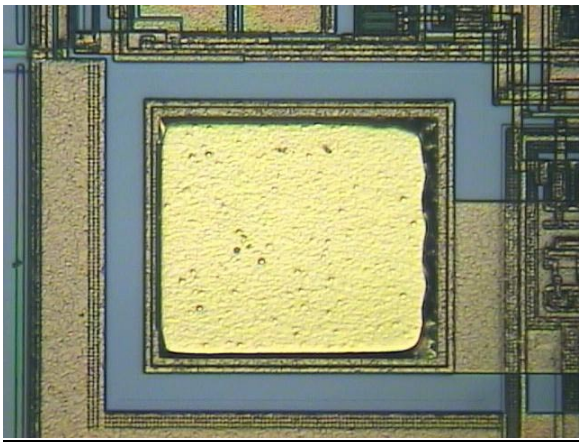
Fig. 6. Close-up photo of an electroless (Ni-Au) plated pad.

This immersion plating process is fairly benign to most CMOS devices and rarely requires any photoresist masking step. The process is commonly employed for bumping RFID and Smartcard chips for flip chip assembly onto flexible inlets - an application that is extremely cost sensitive. Bump height, however, is limited due to the tendency of the plated pads to mushroom outward with increasing plating times.

The present trend towards all copper interconnect at the IC level, instead of aluminum, may make UBM a thing of the past, since the Cu-pads are expected be finished with a thin Ni-Au layer. An alternative method, capable of producing tall columnar-shaped bumps with high aspect ratios on whole wafers, involves an electroplating process. With this technique a copper seed layer is first sputter deposited across the wafer's surface followed by a thick photoresist layer that is then exposed and developed creating openings above the pads into which copper posts are then electroplated. The bump height is determined by the thickness of the confining photoresist. The copper seed layer is later etched away after stripping the photoresist from the wafer. High aspect copper bumps of this type may also be plated on quartz carriers and later transferred to the wafer using a decal approach [4].

In summary, tall conductive columns may be added to ASIC chips at either the die-level or wafer-level using a variety of means. These tall bumps aid in compensating for CTE mismatch between the detector and ASIC chip and lower the capacitance between surfaces. This later characteristic has been identified as a potential advantage for improving energy resolution of hard x-ray sensors.

V. HEFT CdZnTe PIXEL DETECTOR ASSEMBLY

Energy resolution of hard x-ray CdZnTe sensors can be adversely affected by an increase in input capacitance developing between the anodes of the detector and plane of an ASIC preamplifier chip when the parts are mounted too close together. This problem is more likely to occur with parts assembled using indium bump bonding when separation distances between planes are on the order of 8-15µm. To compensate, the anode pads may need to be decreased in size and surrounded with a biased grid-ring in the gap between anodes to steer the charge hitting the surface between pixels towards the anode, thereby minimizing charge loss in the gap.

This type of anode design was implemented in a recent iteration of a CdZnTe detector developed at the California Institute of Technology for the *High-Energy Focusing Telescope (HEFT)*, which is scheduled for a balloon-launched experiment sometime in 2004 [5]. The detector consisted of a 24 X 44 pixel 'gridded' anode pattern, illustrated in Fig. 7, that was attached with indium bumps to a custom, low noise, ASIC chip optimized to achieve low threshold and good energy resolution. Due to manufacturing limitations on the

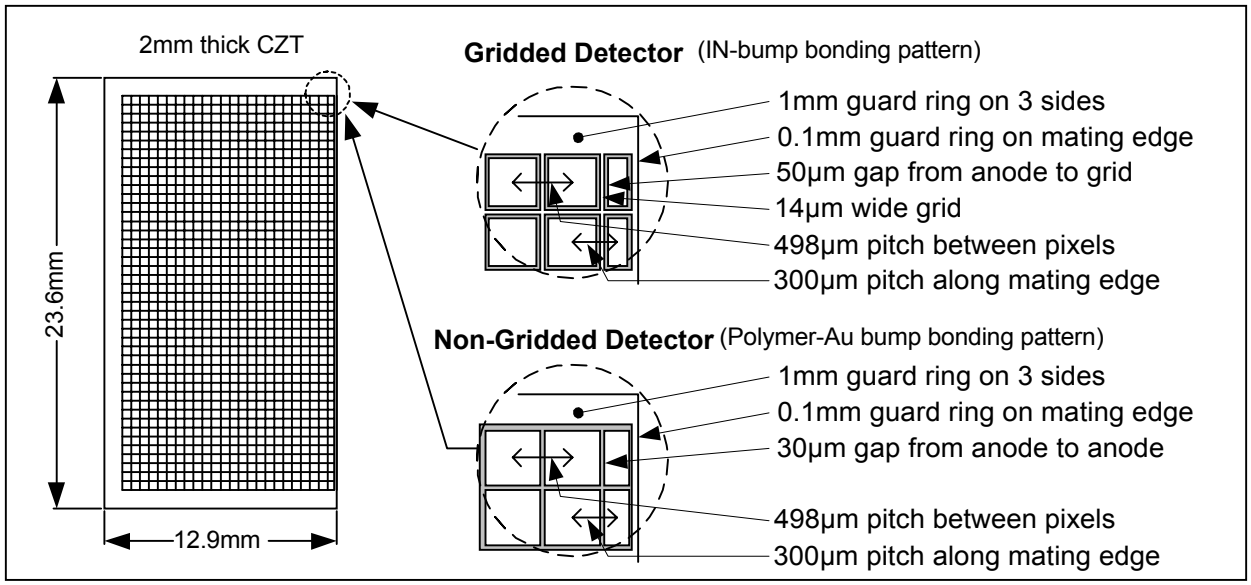

Fig. 7. Anode plane patterns. The gridded pattern at the top is designed for indium bump bonding to minimize the anode contact size and input capacitance. The no-grid pattern at the bottom is designed for bonding with conductive epoxy and gold stud bumps, which are 4-5 times taller than indium bumps. Both patterns contain a mating edge, where the last row of pixels and the guard ring are contracted for a second detector to be placed side by side.

maximum size for single-crystal CdZnTe material with high uniformity and the VLSI readout chip, the detector was designed in two parts, intending to be abutted together to form a larger 48 X 44 array format.

A second detector was later developed for attachment to the same custom readout chip using the polymer flip chip attachment process as discussed earlier. Since the separation distance between planes was expected to increase from 10-12µm to approximately 40µm, with the addition of single-height Au-stud bumps on the ASIC readout chips, the grid was removed and the pads enlarged while still maintaining a low input capacitance. The modified detector anode pattern (without the grid) is also included in Fig. 7. A comparison between the first and second detector designs indicated a 7-11% difference in low and high energy spectral line widths, even at the same pad pitch, due to the allowable increase in pad size and elimination of the grid as a path for current leakage on the surface. A detailed report of this comparison may be found in reference [5].

Fig. 8 is a photograph of a portion of the second detector populated with epoxy bumps on thin-film platinum metal. The bumps that are located on the square pads are spaced at 498µm pitch and range from 130-140µm in diameter and 25-27µm in height. The epoxy used in this assembly (P/N E4110-PFC) is manufactured by Epoxy Technology Inc., Billerica, MA, and exhibits an average shear strength of 40 grams for bumps measuring 100µm in diameter and 30µm height.

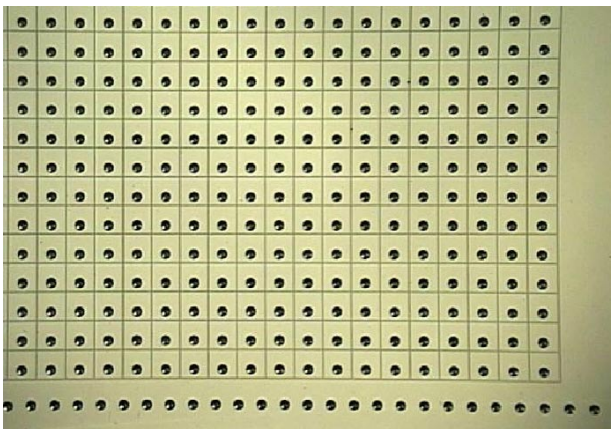

Fig. 8. A portion of a 24X44 CdZnTe pixel-array with conductive epoxy bumps spaced 498µm apart. The bumps are purposely offset from the center-point of each pixel.

After assembly the parts were cured overnight at 70°C to achieve maximum electrical conductivity for this low temperature. Due to the stringent requirement for minimizing input capacitance, any contact between the conductive epoxy and the ASIC chip pads needed to be strictly avoided. This was accomplished by adjusting the stencil printing parameters until the wet epoxy bump height measured approximately half the height of the Au-stud bumps. When the epoxy-bumped detector was aligned and placed onto the Au-stud bumps of the ASIC chip, the weight of the CdZnTe material was sufficient to cause the stud bumps to fully penetrate the epoxy and rest against the surface pads of the detector. At any locations where there were missing

or significantly undersized Au-stud bumps, no contact was possible (refer to Figs. 9 and 10)

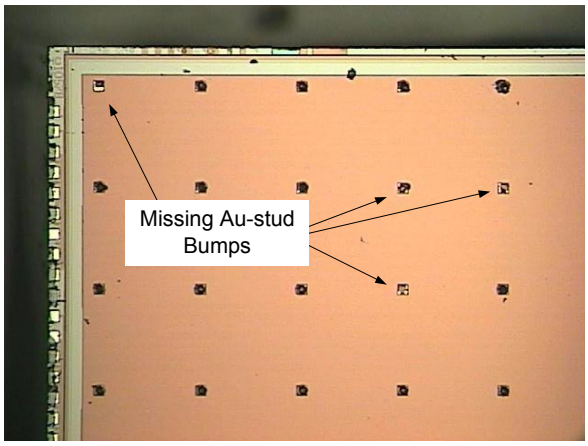

Fig. 9. A portion of the ASIC readout chip indicating locations of missing Au-stud bumps contributing to non-contact with the detector pads.

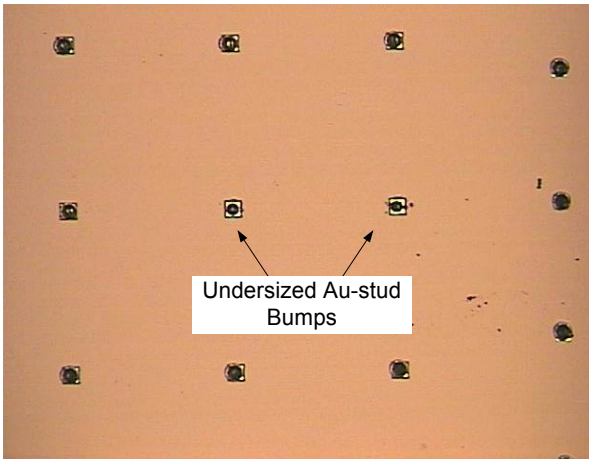

Fig. 10. A portion of the ASIC readout chip indicating locations of undersized Au-stud bumps contributing to non-contact with the detector pads.

The total connectivity for all 1056 possible connections was 1003 or 94.98%, but could not be normalized with respect to the stud bump presence or height, since an accurate map of the ASIC chip bump heights was not made prior to the assembly. Upon viewing the assembled detector from the sides, however, it was apparent that this process was successfully adjusted for contacting only half of the single stud-bump's height, as shown in the side-view of Fig. 11.

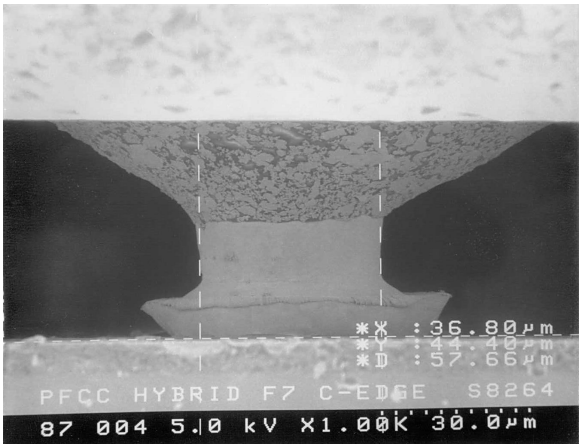

Fig. 11. SEM image of a single Au-stud bump, centered within and connecting to a silver filled, conductive epoxy bump. Note that the epoxy does not reach the surface of the bottom VLSI chip.

Mechanical integrity of the final assembly was dependant upon the arrayed epoxy bonds, supplemented by the application of a small amount of RTV-silicon at each corner of the detector, since no underfill epoxy was permitted for this assembly. The approximate CTE match between the materials being assembled with the conductive epoxy has proven sufficient to allow the finished device to operate reliably at near-zero temperatures.

VI. CONCLUSION

As indicated in the introduction of this article, this technology is presently limited to a minimum pad pitch of approximately 100µm. As Au-stud bump or copper plated column diameters decrease and conductive materials and application techniques improve, it is expected that this type of flip chip mounting technology may soon be extended to pad pitches below 50µm. Applications that are presently dependant upon indium bump bonding may then be able to substitute conductive epoxy bumps as a less expensive alternative.

VII. ACKNOWLEDGEMENTS

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