MEMS Assembly and Wafer Level Packaging – Adapting New Applications to Stencil Printing Technology

Low temperature polymer assembly for fragile MEMS devices and wafer level epoxy coatings are two emerging applications well suited for screen and stencil print processing.

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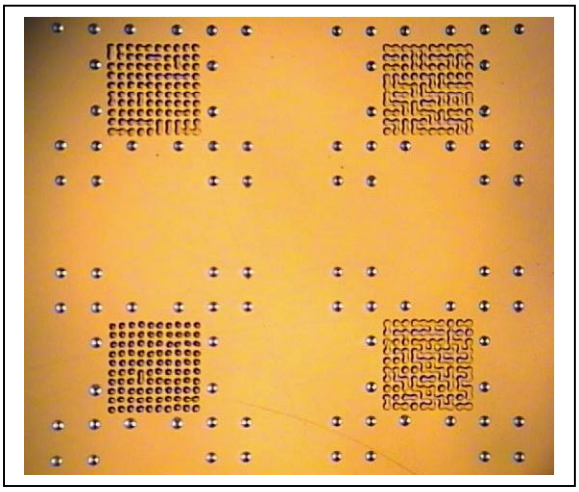
Optoelectronic interconnection has depended upon polymer adhesives since its inception. Epoxy materials are commonly employed for the attachment of lenses on the ends of fiber optic cables, encapsulation or protective coatings, and for die attach of laser diodes to various heat dissipating substrates, to name only a few. MEMS devices and sensor components also represent an emerging new market that will depend heavily on epoxies for assembly in years to come. In many instances, the importance for cleanliness and low temperature processing precluded consideration of solder attachment. Epoxy materials are typically applied within individual packages using automatic dispensers, but the intense commercial need to reduce cost is pushing the industry to develop wafer level packaging alternatives. Wafer level packaging represents the maximum achievable economy-of-scale, depending of course on die size verses wafer size and die yield. Though dispensing technology has achieved significant innovation and improvement over the past decade, the dispensing rates are not expected to be fast enough for processing whole wafers. The issue is similar to the problem facing gold-wire stud bump bonding. Wire bond technology has improved dramatically over the years and bond rates approaching 20 connections per second may soon be achievable. Even at these rates, a single LED or RFID wafer with 400K bond pads could consume an entire production shift of machine-time. A more practical process involves depositing epoxy bumps on the surface of whole wafers using a stencil-printing technique.

Screen and stencil printing technology has been advancing over the years also. Both stencil and screen manufacturing materials and equipment have matured along with the electrically conductive and non-conductive (dielectric) epoxy materials specifically tailored for this type of processing. Assembly techniques are constantly being driven and adapted for the varied applications that appear limited only by the imagination of MEMS and sensor designers. For example, one client needed to assemble a MEMS mirror array on a silicon substrate with an integral mechanical stop on the surface of the substrate. The solution involved a double-printing process, wherein a pattern of 5-micron high dielectric epoxy bumps were first stencil printed and cured, followed by a separate print depositing an outer pattern of electrically conductive epoxy bumps for attaching the mirror array to the silicon surface (Figure 1). Achieving the required 5-micron bump height was a matter of choosing the right combination of stencil aperture and printing parameters for the particular viscosity of the dielectric epoxy used. Though never previously attempted, the subsequent print of the conductive epoxy bumps on the same surface proved fairly simple in practice. The conductive epoxy in this case was a b-staged, solvent-based, thermo-plastic material that needed to withstand the water sprayed on the surface during the dicing operation. A variety of b-staging cure cycles were tested to find the optimal trade-off between bump cohesiveness, capable of withstanding the wafer dicing operation, yet still containing sufficient solvent to be compliant enough to enable the devices to be subsequently thermo-compression bonded to the mirror array.

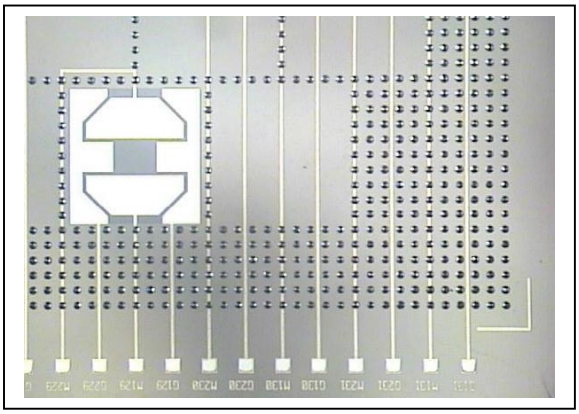
Figure 1: MEMS mirror mounting substrate with stencil printed, conductive and dielectric epoxy patterns.



Another 3D MOEM mirror array was designed for analog beam steering. The unit used a complex feedback technique for mirror control and required accurate placement of the mirror cells in 3-axis. The Z-height was to be controlled by a soft placement technique onto a tightly packed pattern of conductive epoxy bumps that would merge into a contiguous conductive thin film. The MEMS mounting surface included regions with very thin, fragile walls separating adjacent mirror cells. In these sections only a

single row of bumps were deposited to prevent any epoxy spreading into the cells interior region and potentially interfering with the mirror's movement (Figure 2). After experimenting with various stencil apertures and placement pressures, an optimum combination was found that achieved the desired film characteristics without excessive squeeze-out that could interfere with the movement of the 3-axis mirrors. In this example, over 40,000 bumps were required per doublet-cell. The stencil printing process required only a few seconds to perform this process step, yielding a near perfect array of uniform conductive bumps. Attempting to deposit this pattern using an automatic dispenser would have consumed too much time, and the epoxy would have begun to set-up before the pattern could be deposited and transferred into the placement machine. Many low temperature curing (< 100°C) conductive epoxies are characterized by a short pot-life and begin to harden within a few hours, placing a restriction on the processing cycle-time.

Figure 2: MOEM test substrate illustrating conductive epoxy spreading pattern.



As indicated earlier, wafer level processing is also a good candidate for screen and stencil print processing. Polymer Assembly Technology, Inc. is located within the same building owned by Epoxy Technology Corporation of Billerica, MA, and has been co-developing wafer coating processes for their experimental epoxy materials. Recent examples included aluminum-filled epoxy coatings for fingerprint identification chips and boro-nitride filled coatings for chip scale packaging (CSP) applications (Figures 3, 4 and 5). The later application provides both an alpha-particle barrier and thermally conductive path for removing heat from flip chip mounted devices.

Figure 3: CSP epoxy coating test pattern (smallest apertures are .005" on .008" centeres)

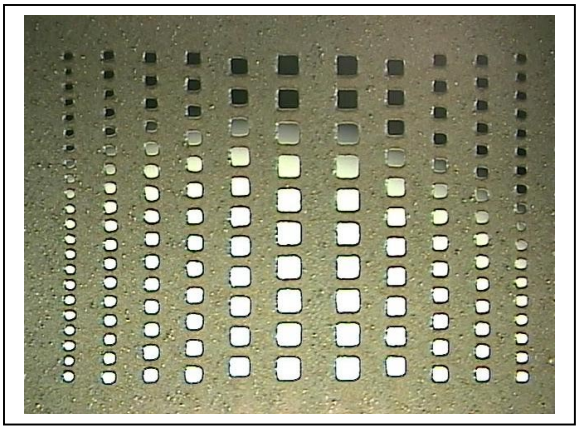


Figure 4: Wafer level epoxy coating with alpha-particle protection and thermal absorption.

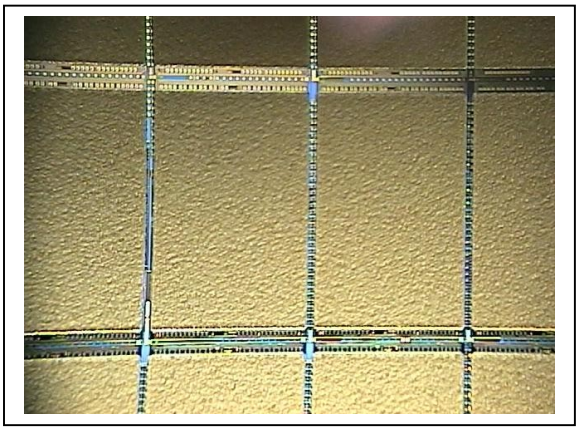
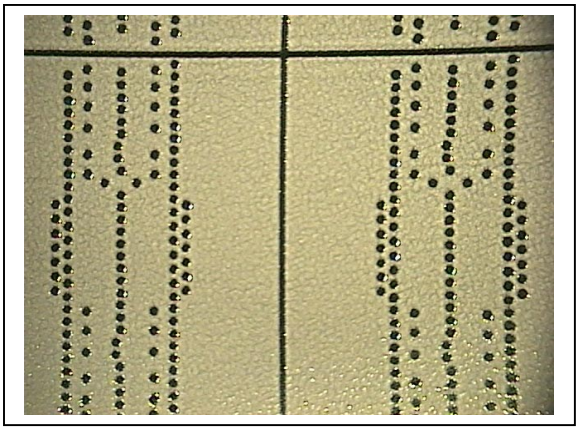


Figure 5: Wafer level epoxy screen print coating.



Research is presently being directed at incorporating nanoscale materials within polymer resins. Carbon particles, for instance, may be stencil printed through smaller apertures than traditional silver-flaked conductive epoxies, which tend to agglomerate and clog stencil apertures smaller than 75-microns diameter. With respect to flip chip assembly, the minimum pitch between

printed epoxy bumps is presently limited to around 125 microns, because of this problem. Nano-sized silver particles are available and may eventually resolve this problem, but are too expensive at present. Therefore, carbon particles are being investigated as a lower cost substitute. Nanoscale carbon can be engineered in a variety of shapes with differing properties that are only just beginning to become understood and developed into useful materials for electronic applications. Though nanotubes and molecular "self-assembly" is the current focus of many research labs, other material properties may soon be exploited for epoxy coatings applied on future wafers using simple low-cost screen and stencil print techniques.

*This article was written by James Clayton, President at **Polymer Assembly Technology, Inc.** For further information, call 1-978-667-0071 or visit www.polymerassemblytech.com.*